REMARKS

Claims 48-124 are pending. In the Office Action dated August 20, 2007, the Examiner objected to claim 48 for informalities and rejected claims 48-124 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,477,614 to Leddige et al. ("Leddige") in view of U.S. Patent No. 5,388,265 to Volk ("Volk") and further in view of U.S. Published Application No. 2005/0177755 to Fung ("Fung").

Disclosed examples of the invention include memory modules having memory hubs connected to a plurality of memory devices. The memory hub includes an activity sensor that monitors the amount of activity of the memory module, and a power controller that is coupled to the activity sensor. The power controller directs the memory module to a reduced power state when the module is not being used at a desired level. See Abstract. Insofar as the activity sensing and resulting power management occurs in the memory module itself, the disclosed power-saving techniques can be applied selectively to each memory module, and it is applied to all of the memory devices in the module and not just the memory hub containing the power controller. This selective application is in contrast with conventional systems that are either implemented across an entire system for example, by placing a system in a standby mode, or that are implemented in only the device or integrated circuit containing the power controller. See ¶ 33. For example, using the disclosed system, a first memory module having a first range of addresses that are frequently accessed can remain operating at full power and capability while all of the memory devices in a second memory module having a second range of addresses that are less frequently accessed can operate at reduced power and capability.

In another embodiment of the invention, the module power controller places the memory module in a reduced response mode by limiting the response of the memory module to memory commands. For example, the module power controller may mandate idle intervals between the memory module's responses to memory commands. In still another embodiment of the invention, an activity sensing device in a computer system containing the memory system monitors memory commands directed to the memory module. The module power controller may then direct the memory module to a reduced power state when the output of the activity sensing

device indicates the memory module has not received a desired number of memory commands for a predetermined time period.

U.S. Patent No. 6,477,614 to Leddige *et al.* has been cited for disclosing a computer system having a processor, an input device, an output device, a memory controller, and a plurality of memory modules coupled to the memory controller and having memory devices mounted on an insulative substrate. Applicants acknowledge that computer systems having these components are well known, and, in fact, used in virtually all personal computer systems. However, as the Examiner acknowledges, the Leddige *et al.* patent fails to disclose an activity sensing device to monitor the activity of the memory module, and a module power controller operable to direct the memory devices in the memory module to a reduced power state responsive to the output of an activity sensing device.

U.S. Patent No. 5,388,265 to Volk describes an integrated circuit floppy disk controller ("FDC") that includes a activity monitor and power management circuit for reducing the power consumed by the FDC when activity falls below a certain level. However, the FDC 400 (Figure 4) does not control or adjust power for any other device or integrated circuit; it only controls its own power consumption. For example, the Volk specification states:

> In the currently preferred embodiment, the power management logic supports two power down modes: direct power down and automatic power down. Direct power down occurs when programming action directly results in the *powering down the chip* with little or no delay or dependence on other factors (i.e., chip activity). Automatic power down results when power management logic monitors the FDC for certain conditions and according to a previously programmed mode.
>
> As soon as the auto power down mode is enabled, a program minimum delay timer (see Fig. 11) begins counting. If the motor enables are not active after the predetermined time has been reached by the timer in the FDC is idle, then the power management logic *powers down the FDC.*

[Column 11, lines 1-17, emphasis added].

Therefore, if the activity monitor and power management circuit was used in applicant's memory hub in place of applicant's activity monitor and power management circuit,

the power management circuit would only control the power consumed by the memory hub. Significantly, unless the power management circuit departed from the teachings of the Volk patent in a manner not taught by any of the cited references, it would not control the power consumed by the memory devices connected to the memory hub. Yet the power consumed by the memory devices would undoubtedly be significantly greater than the power consumed by the memory hub. Furthermore, although the Volk patent describes an integrated circuit floppy disk controller ("FDC") that includes a activity monitor and power management circuit, it fails to disclose an activity sensing device that monitors memory commands directed to a memory module. The Volk patent also fails to disclose or suggest limiting the response of a memory module to memory commands, such as by mandating idle intervals between responses, in order to control the power consumed by a memory module.

U.S. Patent Publication No. 2005/0177755 to Fung has been cited for disclosing the use of a temperature sensor to sense the level of activity of a circuit, as recited in some of the dependent claims. However, the Office Action does not contend that the Fung patent contains any teachings that are missing from the teachings of the Volk patent or the Leddige *et al.* patent.

Turning, now, to the claims, independent claim 48, as amended, specifies a memory system comprising a memory controller and a plurality of memory modules coupled to the memory controller through a memory bus. Each of the memory modules include a plurality of memory device is disposed on an insular to substrate, and a memory hub disposed on the insular to substrate and operably coupled with the memory devices. The memory hub includes an activity sensing device, and a module power controller that is responsive to the output of the activity sensing device if the activity sensing device provides an indication that the activity is not of a desired level. Unlike the power controller disclosed in the Volk patent, the claimed module power controller directs the *memory devices* of the memory module containing the module power controller to a reduced power state, although it may also direct the memory hub containing the power controller to a reduced power state, like the power controller disclosed in the Volk patent. As explained above, none of the cited references, taken alone or in combination, suggest a memory system as recited in claim 48.

Claim 74 is directed to a computer system including a processor, an input device operably connected to the processor, an output device operably connected to the processor, and

the memory system of amended claim 48. Claim 74 therefore patentably distinguishes over the cited references for at least the same reasons that claim 48 patentably distinguishes over these references.

Amended claim 100 is directed to a method of controlling power in a plurality of memory modules associated with a system. The method includes individually measuring activity in each of the memory modules in response to memory commands from the system and at least some of the memory modules. A determination is then made when each of the memory modules is inactive based on a lack of measured activity in response to non-refresh memory commands from the system. Finally, the memory devices in at lease one of the memory modules is directed into a reduced power state when it is determined that the activity of the memory module is not of a desired level.

New claim 125 is a combination of prior claim 48 and dependent claim 70. The claims specifies a memory system comprising a memory controller and a plurality of memory modules coupled to the memory controller through a memory bus. Each of the memory modules include a plurality of memory device disposed on an insulativesubstrate, and a memory hub disposed on the insulative substrate and operably coupled with the memory devices. The memory hub includes an activity sensing device, and a module power controller that is responsive to the output of the activity sensing device if the activity sensing device provides an indication that the activity is not of a desired level. The claimed module power controller directs the memory module containing the module power controller to a reduced power state by limiting the response of the memory module to memory commands. As explained above, none of the cited references, taken alone or in combination, suggest a memory system as recited in claim 125.

New claim 127 is the combination of prior claim 74 and the pending claims 96. It essentially recites the memory system of new claim 125 in the context of a computer system, and is therefore patentable for at lease the same reason that new claim 125 is patentable.

New claim 129 is the combination of prior claim 74 and dependent claim 84. Claim 129 specifies a computer system containing a processor, an input device operably coupled to the processor, an output device operably coupled to the processor, and a memory system. The memory system includes a memory controller and a plurality of memory modules coupled to the

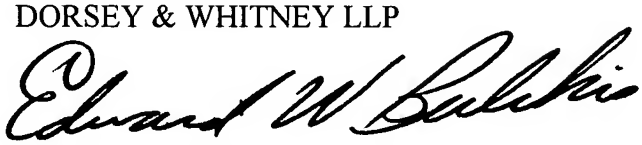
memory controller through a memory bus. Each of the memory modules include a plurality of memory device disposed on an insulative substrate, and a memory hub disposed on the insulative substrate and operably coupled with the memory devices. The memory hub includes an activity sensing device monitoring memory commands directed to the memory module. The activity sensing device generates an output corresponding to module activity based on the monitored memory commands. Finally, a module power controller directs the memory module containing the module power controller to a reduced power state responsive to the output of the activity sensing device indicating activity of the memory module containing the module power controller is not of a desired level. As explained above, none of the cited references, taken alone or in combination, suggest a computer system as recited in new claim 129.

The claims that are dependent on the above-discussed independent claims also patentably distinguish over the cited references because of their dependency on patentable independent claims and because of the additional limitations added by those claims.

All of the claims remaining in the application should now be allowed. Favorable consideration and a timely Notice of Allowance are earnestly solicited.

Respectfully submitted,

DORSEY & WHITNEY LLP



Edward W. Bulchis
Registration No. 26,847
Telephone No. (206) 903-8785

EWB:dms

Enclosures:
Postcard
Check
Fee Transmittal Sheet (+copy)

DORSEY & WHITNEY LLP
1420 Fifth Avenue, Suite 3400
Seattle, WA 98101-4010
(206) 903-8800 (telephone)
(206) 903-8820 (fax)

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